AMENDMENTS TO THE SPECIFICATION

On page 1, please amend the first section starting on line 4 as follows:

REFERENCE TO PRIOR ~~APPLICATION~~ APPLICATIONS

The current application is a divisional of co-pending U.S. patent application serial no. 09/966,559, filed on 09/27/2001, which claims the benefit of U.S. ~~priority to co-pending~~ provisional application serial number 60/235,563, filed on 09/27/2000.

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The U.S. Government has a paid-up license in this invention and the right in limited circumstances to require the patent owner to license others on reasonable terms as provided for by the terms of DR9A901000-01 awarded by the U.S. Army BMDO/SMDC.

Please amend the paragraph starting on line 19 of page 8, and ending on line 9 of page 9 as follows:

Figure 3 shows one embodiment of the present device structure. The AlGaN/GaN heterostructure was grown by MOCVD on a sapphire substrate 30. A roughly 50 nm AlN buffer layer 31 ~~(not shown)~~ was first grown on the substrate 30. The next step was to apply the active layer. This included the deposition of an approximately 1 μm insulating GaN layer 32 and a roughly 50 nm n-GaN layer 33 ~~(not shown)~~ with an estimated doping level between $2x10^{17}$ cm^{-3} and $5x10^{17}$ cm^{-3}. Next, a barrier layer was applied. In this case, the heterostructures were capped with a roughly 30 nm $Al_{0.2}Ga_{0.8}N$ barrier layer 34, which was doped with silicon to approximately 2×10^{18} cm^{-3}. The measured Hall mobility was about 1,180 cm^2/V-s and the sheet carrier concentration was about 1.15×10^{13} cm^{-2}. Finally, prior to transistor fabrication, a roughly 15 nm SiO_2 layer 36 was applied onto the heterostructures using PECVD. The thickness was verified with capacitance-voltage (C-V) measurements on device wafers with and without the SiO_2 layer 36.